REMARKS

Reconsideration of this application, in view of the foregoing amendments and the following remarks, is respectfully requested.

Claim Rejections - 35 USC §102

Claims 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 5,956,748, New. Applicants respectfully traverse these rejections.

To anticipate a claim under 35 U.S.C. §102(e), the reference must teach each and every limitation of the claim. *See* M.P.E.P. §2131. New does not teach each and every limitation of claim 1. As to claim 1, the Examiner has stated that "a **plurality of** valid logic circuits, **each** associated with a **corresponding one** of the plurality of **entries of the buffer** (figure 2, **elements 241 and 240** act as valid logic circuits by enabling the read and write operations)" (Emphasis added). Applicants respectfully request the Examiner to note that the particular element of claim 1 recites the following:

1. a **plurality** of valid logic circuits;
2. **each** associated with a corresponding one of the plurality of entries of the buffer.

Thus claim 1 recites that each one of the plurality of entries is associated with a distinct valid logic circuit. This means that there can be as many valid logic circuits as there are entries in the buffer. The Examiner has cited elements 240 and 241 of New as valid logic circuits **each associated with a corresponding entry of the buffer**. Applicants respectfully point to the Examiner that, elements 240 and 241 control read and write operation for the entire buffer 202 and do not control the operation of each individual entry of the buffer 202 and are definitely not associated with a particular entry of the buffer 202. These circuits assert FULL and EMPTY flags based on the crossover of read/write addresses to prevent the overlapping of read/write operation based on different clocks. When FULL flag is asserted, the read operation proceeds regardless of the validity of data in the memory location until the FULL flag is de-asserted. The

assertion of FULL flag is based on a determination of a potential overlapping of read/write addresses. This determination is made by respective comparators 207 and 208 based on current read/write addresses CURRENT_WA and CURRENT_RA, which are synchronized for respective clocks as SYNC_WA and SYNC_RA for a synchronized comparison. This means that the read operation always follows the write operation and elements 240 and 241 prevent the read operation from running ahead of the write operation (*see* figure 2 and corresponding description). Therefore, New only determines the validity of data in any location by comparing current write and current read addresses to prevent accidental reading a memory location that has not been written yet.

In a complete contrast, claim 1 recites individual valid logic circuits associated with each one of the locations in the memory. Thus, the read/write operation in the recited structure does not depend upon read/write addresses but on determination of the status of a valid logic circuit associated with a particular memory location. In such case, read operation can freely scan the entire buffer regardless of the current write address and read data from the particular memory location based on the indication of the respective valid logic circuit. Further, it does not require synchronization of read/write addresses for respective clocks. New does not teach this limitation.

As to the write valid latch in each of the valid logic circuits, the Examiner has cited elements 214 and 212. As explained above, first, New does not disclose valid logic circuitry associated with each one of the entries of the buffer. Second, the cited latches 212 and 214 are part of a feedback loop comprising comparators 207 and 208, AND gates 221 and 222, and multiplexers 223 and 224. The feedback loop controls the respective FULL/EMPTY flag based on a comparison of read/write addresses. When these addresses are equal, the respective comparator provides a logic high output, which is routed through the multiplexer to respective read/write control circuit to prevent the operation. Again, Applicants respectfully point that this operation is based on address comparison and is not associated with individual entry of the buffer 202. In contrast, claim 1 recites write valid latch associated with each one of the locations in the memory. New does not teach this limitation. Similarly, New does not teach individual read valid latch for each one of the locations in the memory as recited in claim 1.

As to the reset logic for resetting the write valid latch, the Examiner has cited the combination of elements 207, 221, and 223 and stated that "... figure 2, elements 207, 221, and 223 act together to reset the logic in the latch as read in col. 7, lines 11-22". Applicants respectfully request a careful reading of the claim element. Claim 1 recites reset logic for resetting the write valid latch responsive to the read request signal. According to the recited element, the write valid latch gets rest responsive to the **read request signal**. In contrast, the combination of cited element actually resets the FULL signal only upon detecting an equality in SYNC_RA signal and CURRENT_WA signal. The read control 204 continuously reads data from the buffer 202 and asserts read signal for every read operation; however, the combination of cited elements in New does not assert a reset signal on every read signal – it asserts reset only when it detect and equality of addresses (*see* col. 7, lines 26-46). Accordingly, New does not teach resetting the write valid latch responsive to the read request signal as recited in claim 1. Similarly, New does not teach set logic for setting read valid latch responsive to the write request as recited in claim 1.

Claims 2-4 depend from claim 1 and are patentably distinguishable from New for at least the same reasons as claim 1.

Further as to claim 3, the Examiner has cited element 207 as the first edge detector and elements 210 as the synchronizer circuit as recited in claim 3. Applicants respectfully point to the Examiner that first, the element 207 is not an edge detector, it is a comparator, second, the comparator 207 does not detect a transition of the read request signal instead it compares read and write addresses. The read signal in New is used to increment a read address counter 206, which provides the address of the location currently being read to the comparator 207 as SYNC_RA. Furthermore, the Examiner has cited the sync engine 210 as synchronization circuit having an input coupled to the first edge detector as recited in claim 3. Applicants respectfully point to the Examiner that first, the sync engine 210 is not coupled to comparator 207, second, in rejecting claim 1, the Examiner has cited latch 214 as the write valid latch; however, are careful reading of claim 3 will reveal that claim 3 recites that the first synchronizer circuit has an output coupled to a reset input of the write valid latch. However, New does not show that the sync engine 10 has an output coupled to the latched 214 as recited in claim 3. Accordingly, New does

not teach each and every limitation of claim 3 and claim 3 is further patentably distinguishable from New.

Similarly, for claim 4, the Examiner has cited the element 208, which is also a comparator and compares the current read address CURRENT_RA with the current write address SYNC_WA and does not detect the transition of write signal. In fact, neither of the comparators 207 and 208 receives the read/write signal from corresponding read/write control 204/203. Accordingly, claim 4 is further patentably distinguishable from New.

Regarding claim 5, Applicants respectfully request the Examiner that in light of above explanation with reference to claim 1, please take a particular note of steps reciting setting/resetting read/write bits associated with first and second one of the plurality of entries. Claims 5 recited read/write valid bits associated with each one of the memory entries. As explained above, New does not teach this limitation. Accordingly, claim 5 is patentably distinguishable from New for at least this and other reasons stated above with reference to claim 1.

Claims 6-9 depend from claim 5 and are patentably distinguishable from New for at least the same reasons as claim 5.

Claim Rejections - 35 USC § 103

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over New in view of U.S. Patent 5,487,092, Finney et al. (Finney). Applicants respectfully traverse this rejection.

Claim 9 depends from claim 5, which has been distinguished from New for failing to disclose read/write valid logic circuits associated with each of the entries of the memory. Therefore the combination of New and Finney et al. cannot render claim 9 obvious.

In the previous response Applicants respectfully pointed to the Examiner not only it will not be obvious to include idle symbols in New but in fact, one skilled in art will consider it as a waste of data bandwidth and in fact, New teaches away from using any other means for the synchronization of read and write operations besides the sync engine 210. In response to the rejection of claim 9 in the previous office action over New in view of Finney et al., Applicants

very clearly described differences between New and Finney et al. and showed that there are significant differences between teachings of New and Finney et al. and that teaching of these references cannot be combined.

However, in rejecting claim 9, the Examiner has stated that "*the differences between New and Finney with regard to the inserting of the idle symbol are irrelevant)*" (Emphasis added). Applicants respectfully point to the Examiner that there are three basic criteria to establish a *prima facie* case of obviousness under 35 U.S.C. §103(a). First, there must be some suggestion or motivation in the cited references to modify or combine their teachings; second, there must be reasonable expectation of success; and third, the prior art references must teach or suggest all the claim limitations. *See* M.P.E.P §2142.

Further Applicants respectfully point to the Examiner that M.P.E.P. clearly states that the "fact that references can be combined or modified is not sufficient to establish *prima facie* case of obviousness." Furthermore, "the proposed modification cannot render the prior art unsatisfactory for its intended purpose." *See* M.P.E.P. §2143.01. Applicants have clearly established that neither of the cited references teach, suggest, or provide motivation to combine their references with regard to idle symbols and that even after combining the references, New cannot use idle symbols for synchronization as taught by Finney et al. In response, the Examiner has stated that the differences are "irrelevant." Applicants respectfully point to the Examiner that not only these differences are relevant but in fact, the proof of these differences is actually required by the rule to prove lack of suggestion or motivation to modify or combine teachings of references as explained above. Applicants have established that these references cannot be combined and these references do not provide motivation for or suggest combining their teachings. Accordingly, claim 9 is further patentably distinguishable from the combination of cited references.

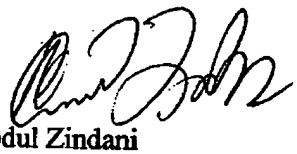
Claim10 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,233,221 B1, Lowe et al. (Lowe) in view of New. Applicants respectfully traverse these rejections.

As to claim 10, the Examiner has cited New for disclosing the transmit clock generator and various elements as recited in claim 1. Applicants have explained above with reference to claim 1 that New does not disclose the clock unit as recited in claim 10. Accordingly, claim 10 is patentably distinguishable from the combination of cited references for at least the same reasons as given for claim 1.

Claim 15 has been rejected in the manner of claims 3 and 4. Accordingly, claim 15 is patentably distinguishable from the combination of cited references for at least the same reasons as claims 3 and 4.

Applicant believes this application and the claims herein to be in a condition for allowance. Should the Examiner have further inquiry concerning these matters, please contact the below named attorney for Applicant.

Respectfully submitted,



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